REMARKS

In an Office Action mailed February 22, 2005, pending claims 1-47 were examined. Claims 1-2, 5, 10-13, 17-25, 36-44 and 46 were rejected and claims 3-4, 6-9, 14-16, 26-35, 45 and 47 were objected to for being allowable if rewritten in independent form with all of the base claim limitations. In response, Applicants are herein amending claims 1, 3, 4, 7, 8, 10-13, 23, 25, 27, 30, 31, 36-38, 40, 41, 43, 44, canceled claims 2, 6, 24, 26, 29 and 45, and respectfully requesting the reconsideration and allowance of claims 1, 3-5, 7-23, 25, 27, 28, 30-44, 46 and 47, thereby placing the application in condition for allowance.

Claims 1, 2 and 23 were rejected under 35 U.S.C. 112 second paragraph, for being indefinite in connection with the phrase "at least one of the analog input signal" in claims 1-2 and the phrase "at least one of the analog signal input node" in claim 23. In response claim 1 is amended to recite "at least one of the analog input signal or one of the plurality of reference input signals". As amended claim 1 clearly recites that what is received is at least the analog input signal or one of the reference inputs signals, if not both. Claim 2 is herein canceled with the key limitations incorporated into claim 1 without any ambiguity associated with the recited third capacitor. Claim 23 is herein amended to recite that the capacitance elements are coupled to the analog signal input node or the reference input node, or to both. All potential ambiguity has been removed. Therefore, withdrawal of the rejection of claims 1 and 23 under 35 U.S.C. 112, second paragraph, is herein requested.

Claims 1, 2, 5, 10-13, 17-25, 36-44 and 46 are rejected under 35 U.S.C. 102(b) as being anticipated by Garrity et al. (U.S. Patent 5,574,457). In response, Applicants have amended claims independent claims 1, 23, 43 and 44. Claim 1 is herein amended by incorporating the recitals of objected claim 6 and is therefore allowable over Garrity et al. The structural recitals of the A/D converter of claim 1 are readily distinguishable from the switched capacitor gain stage of Garrity et al. Claim 23 is herein amended by incorporating the

recitals of objected claim 26 and is therefore allowable over Garrity et al. Claims 43 and 44 are herein amended. Garrity et al. do not teach or suggest "allowing a user of the system to control a predetermined scale factor" as recited in claim 43. Garrity was stated to teach a selectable scaled factor as Col. 2, lines 53-55 and Col. 3, lines 33-67 were stated to be the basis. However, these sections of Garrity do not teach or suggest selectable scale factors. The gain stages of Garrity are taught as having fixed gain. The gain factor can differ from implementation to implementation, but there is no teaching of a selectable scale factor. The adding or subtracting of a fixed reference voltage is a comparator operation to sequentially determine the digital bits of the analog input. Claim 44 is herein amended to incorporate the recitals of claim 45 which was objected to and therefore claim 44 is placed in condition for allowance. Applicants therefore request the reconsideration and withdrawal of the rejection of claims 1, 5, 10-13, 17-23, 25, 36-44 and 46 on the stated basis.

Allowance of claims 1, 3-5, 7-23, 25, 27, 28, 30-44, 46 and 47 is respectfully requested, thereby placing the application in condition for allowance. Should issues remain that might be subject to resolution through a telephonic interview, the Examiner is requested to telephone the undersigned at (512) 996-6839.

Respectfully submitted,

SEND CORRESPONDENCE TO:

Freescale Semiconductor, Inc.
Customer Number: 23125

By: Robert L. King

Robert L. King
Attorney of Record
Reg. No.: 30,185
Telephone: (512) 996-6839
Fax No.: (512) 996-6854